

PROVED O.G. FIG.

CLASS SUBCLASS

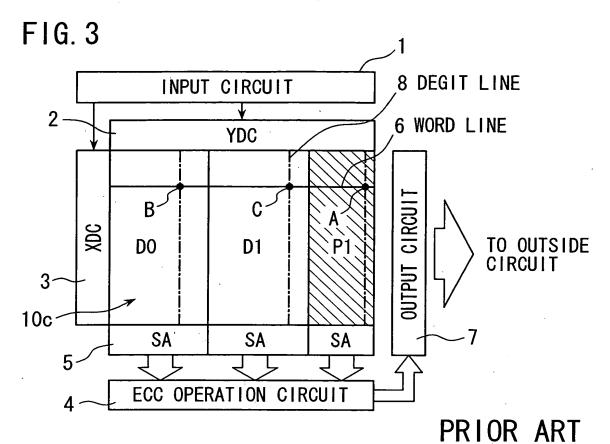
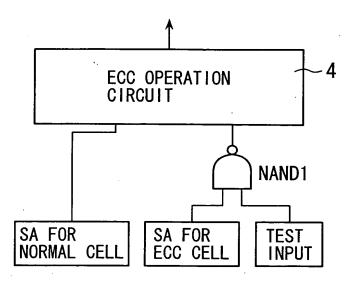


FIG. 4 2a INPUT CIRCUIT 2b 6 WORD LINE YDC YDC OUTPUT CIRCUIT XDC XDC `P1 TO OUTSIDE CIRCUIT **D1** D0 10d 3b-10e SA SA SA 3á 5 ECC OPERATION CIRCUIT PRIOR ART

FIG. 5



WHEN ECC ENABLED: TEST INPUT IS VCC  $\rightarrow$  OUTPUT OF NAND1 DEPENDS ON ECC CELL DATA

WHEN ECC DISABLED: TEST INPUT IS GND  $\rightarrow$  OUTPUT OF NAND1 IS ALWAYS HIGH

PRIOR ART